REMARKS/ARGUMENTS

Claims 1, 4, 6, 8, 10, 14, 15 and 19-21 were pending in the Application. By this amendment, claims 1, 4, 6, 8, 10, 14, 15, 19 and 20 are being cancelled, claim 21 is being amended to improve its form, and new claims 26-30 are being added. No new matter is involved.

In Paragraph 1 on page 2 of the Office Action, claims 14, 15 and 19 are rejected as indefinite. However, such rejection is obviated by the cancellation of claims 14, 15 and 19.

In Paragraph 3 which begins on page 2 of the Office Action, claims 1, 4, 14 and 19-21 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent 5,290,361 of Hayashida et al. in view of U.S. Patent 5,518,624 of Filson et al. In Paragraph 4 on page 3 of the Office Action, claims 6, 8, 10 and 15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hayashida et al. and Filson et al., and further in view of U.S. Patent 4,973,563 of Prigge et al. Such rejection is respectfully traversed with respect to claim 21, particularly as amended herein. The remaining rejections are obviated by the cancellation of claims 1, 4, 6, 8, 10, 14, 15, 19 and 20.

As amended herein, independent claim 21 reads as follows:

> "A regulating method of a storage water used for storage of a silicon wafer in water, wherein the concentration of Cu in the storage water, which is ultra pure water containing a chelating agent and a surfactant, is regulated to 0.01 ppb or less in the form of pit water in a waiting period between steps before a cleaning step in a silicon wafer production process (emphasis added)".

As used in the claim, the expression "storage water" means water in the form of pit water used for storage of a silicon wafer in water in a waiting period between

steps before a cleaning step in a silicon wafer production process. Therefore, the "storage" in the case of the present application is completely different from the cleaning step and the steps after the cleaning step.

It is known in the art that if heat treatment is performed on a wafer without removal of impurities, and especially heavy metals adhering thereto, the impurities adversely affect the electrical characteristics of semiconductor devices. For this reason, a cleaning step for removing impurities is usually provided before the heat treatment. Therefore, detecting and removing contamination of cleaning solution and that of the surface of a silicon wafer after the cleaning step are highly important, and conventionally, techniques for removing such contaminant have been studied (see line 19 of page 2 to line 2 of page 3 of the specification). On the contrary, conventionally, detecting contamination or the like of storage water has not been regarded as very important. Because it has been considered that even if a wafer is contaminated by contaminated "storage water" during storage, the contamination during the storage can be eliminated in a subsequent "cleaning step" for cleaning a wafer.

However, the inventors of the present invention found that even when cleaning is performed, while the concentration of contaminant in cleaning solution is controlled, in order to produce a silicon wafer having a clean surface, a final wafer that has undergone all processing steps sometimes becomes defective in that its oxide dielectric breakdown voltage is degraded (see lines 11-16 of page 3 of the specification). Moreover, the inventors also found that even in the case of a defective wafer having degraded oxide dielectric breakdown voltage, proper cleaning had been performed and therefore impurities had been removed (see line 27 of page 3 through line 4 of page 4 of the specification).

Therefore, the inventors of the present invention analyzed the causes of such degradation of oxide dielectric breakdown voltage, and found that such degradation

is caused by a conventional method of storing a silicon wafer in a step before the cleaning step (see lines 5-10 of page 4 of the specification), and especially, such inventors found that in the case where the concentration of Cu ions in storage water is higher than 0.01 ppb, if a silicon wafer having a hydrophobic surface is stored in the storage water immediately after polishing, the quality of oxide film degrades significantly during a subsequent thermal oxidation step. This results in the occurrence of degradation of oxide dielectric breakdown voltage (see lines 4-11 of page 5 of the specification). Various factors, such as contaminant carried over from preceding steps, can cause contamination of storage water at a low level of Cu ions (see lines 12-14 of page 5 of the specification). Therefore, even if the concentration of Cu ions in a storage water is 0.01 ppb or less at the beginning, the concentration of Cu ions in storage water becomes higher than 0.01 ppb due to contamination by use in storage.

With this background, the advantageous method in accordance with the invention, as set forth in claim 21, was invented by the inventors.

Moreover, because the present invention can constantly regulate the concentration of Cu ions in the storage water to 0.01 ppb or less, methods according to the present invention prevent degradation of oxide dielectric breakdown voltage, which would otherwise occur due to contamination by Cu contained in storage water and which has been a problem in the relation to storage of a silicon wafer in water (see lines 5-9 of page 10 of the specification). Furthermore, because the storage water of the present invention is added to a chelating agent, the water provides more significant effect to eliminate metallic contamination such as Cu (see line 26 of page 14 through line 3 of page 15 of the specification). Furthermore, addition of a surfactant to the storage water improves particle removal performance of the storage water (see lines 12 and 13 of page 6 of the specification). Furthermore, the storage water is preferably used in the form of pit water so as to maintain the

concentration of added surfactant at a certain level (see line 17-19 of page 13 of the specification).

To the contrary, it is stated in Paragraph 3 of the Office Action that "Hayashida et al. teaches storing a silicon wafer in water, wherein the storage water is UPW (ultra-pure water) containing a chelating agent (col. 7, line 61 to col. 8, line 5) and a surfactant (col. 8, lines 11-14) (emphasis added)." As further stated in that paragraph, "Filson et al. teaches high purity water for use in semiconductor processing containing Cu in an amount below 0.005 ppb, ...". Reference is further made to Table II, col. 15. As further stated therein, "As Filson et al. teaches that it is imperative to use water free of all contaminants in semiconductor processing (col. 1, lines 41-50) in order to avoid contamination of substrates, it would have been obvious to use the water of Filson et al. as the UPW used in the method of Hayashida et al.".

Such statements in the Office Action indicate a misunderstanding of the meaning of "storage water" as used in the present invention. The "cleaning or treating" or "treating or rinsing" described in Hayashida et al. has been confused with "storing" in the case of the present invention. "Storage water" is not described in column 7, line 61 to column 8, line 5 of Hayashida, et al., but it is described therein that after a step of "cleaning or treating" surfaces of semiconductors with a surface treating solution, the resulting surfaces are treated or rinsed with ultra-pure water containing a chelating agent. Because the surface treating solution is used for cleaning surfaces of semiconductors (column 1, lines 5-8 of Hayashida et al.), i.e., used in a "cleaning step", the solution is not used for the "storage". And the "treating or rinsing" is the step performed after the cleaning step, which is apparently different from the "storage" performed before the cleaning step. Also, the term "storage water" is not described in col. 8, lines 11-14 of Hayashida et al.,

but only a semiconductor surface treating solution containing surfactants is described therein.

Therefore, Hayashida et al. neither discloses nor suggests the "storage water" and the "storage" in accordance with the present invention. Therefore, even if the high purity water of Filson et al. containing Cu in an amount below 0.005 ppb, and so on, is used as the "UPW" in the method of Hayashida et al., it means that the water is used for rinsing, i.e., used after cleaning, which has no relation to the "storage water" used before cleaning.

Furthermore, although it is described in Hayashida et al. that ultra-pure water (UPW) containing a chelating agent is used for "treating or rinsing" after cleaning, Hayashida et al. does not recognize that there is a problem in the case of storing a wafer in storage water containing Cu at a concentration of higher than 0.01 ppb before cleaning, that even when cleaning is subsequently performed, the oxide dielectric breakdown voltage of the wafer is degraded. Namely, even if a step of "treating or rinsing" a wafer is performed with the high purity water of Filson et al. containing Cu in an amount of 0.005 ppb, and so on used as the "UPW" in the method of Hayashida et al., the oxide dielectric breakdown voltage of the wafer is degraded if the concentration of Cu in the storage water is higher than 0.01 ppb.

Also, because conventionally it has been considered that even if a wafer is contaminated by contaminated "storage water" during storage, the contamination during the storage can be eliminated by a subsequent "cleaning step" for cleaning a wafer, one of ordinary skill in the art does not recognize that the concentration of Cu in the storage water should be regulated.

Moreover, various factors, such as contaminant carried over from preceding steps, can cause such contamination of storage water at a lower level of Cu ions. Therefore, in the case that the concentration of Cu in storage water is not regulated, even if the concentration of Cu in storage water is 0.01 ppb or less at the beginning,

the concentration of Cu in the storage water becomes higher than 0.01 ppb due to contamination by use in storage.

Because neither Hayashida et al. nor Filson et al. describe the "storage water", as noted above, and neither reference discloses or suggests that there is a problem in the case of storing a wafer in storage water containing Cu at a concentration of higher than 0.01 ppb before cleaning, even when cleaning is subsequently performed, the oxide dielectric breakdown voltage of the wafer is degraded. One of ordinary skill in the art cannot arrive at the present invention from Hayashida et al. or Filson et al. Therefore, the present invention is submitted to clearly distinguish patentably over such references.

As previously discussed, claim 21 defines the present invention in a manner which is submitted to clearly distinguish patentably over the art. New claims 26-30 depend, directly or indirectly, from claim 21, and further define claim 21 in terms of limitations similar to those in claims 6, 8, 10, 19 and 20, respectively. Such claims contain all of the limitations of claim 21 and therefore also distinguish patentably over the art.

In conclusion, claims 21 and 26-30 are submitted to clearly distinguish patentably over the art for the reasons discussed above. Therefore, reconsideration and allowance are respectfully requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (213) 337-6846 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
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Date: February 4, 2004

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